



UNITED STATES PATENT AND TRADEMARK OFFICE

Am
UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/081,658	02/22/2002	Thomas L. Stachura	10559-773001/P13943	2123
20985	7590	04/11/2005	EXAMINER	
FISH & RICHARDSON, PC 12390 EL CAMINO REAL SAN DIEGO, CA 92130-2081				PATEL, ANAND B
ART UNIT		PAPER NUMBER		
		2116		

DATE MAILED: 04/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/081,658	STACHURA ET AL.
	Examiner	Art Unit
	Anand Patel	2116

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 07 March 2005.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-7,10-14,16-23 and 26-32 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-3,6,7,12,20,22,23,30 and 31 is/are rejected.
- 7) Claim(s) 4,5,10,11,13,14,16-19,21,26-29 and 32 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Applicant's arguments filed 3/7/05 have been entered and as such claims 8-9, 15, 24-25 have been canceled.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-2, 6-7, 12, 22, 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No 5842027 to Oprescu et al (Oprescu) in view of US Patent No 6601174 to Cromer et al (Cromer).

As per claim 1, Oprescu discloses an apparatus comprising:

- A device having a high power state and a first low power state and a second low power state (column 3, lines 3-15); and
- A power management system (14) configured to transition the device from the high power state to one of the low power states (115) when a signal is detected on the bus (power usage request).

Oprescu fails to disclose a physical layer interface as a part of the system. Cromer teaches:

- An electrically powered physical layer interface (234) to interface between a bus and a network (Network).

The physical layer improves system performance by utilizing the highest performance connectivity technology (column 5, lines 32-37). It would have been an obvious to one of ordinary skill in the art at the time of invention to modify Oprescu by Cromer.

Motivation to modify arises from the improvement in performance gained through the use of a physical layer interface as outlined in Cromer.

- As per claim 2, Cromer discloses an apparatus wherein the bus is a PCI bus (208).
- As per claim 6, Oprescu discloses an apparatus wherein the first low power state is when the device is powered off (115; the revocation of the power usage grant is analogous to shutting down the device).
- As per claim 7, Oprescu discloses an apparatus wherein the second low power state is a state in which the device draws no more than a predetermined amount of current (115; when the interface is switched off, it is not drawing any current).
- As per claim 12, Oprescu discloses a system comprising:
 - A communications device in communication with the bus (14), the communications device comprising:
 - An electrically powered device having a high power state and a first low power state, and a second low power state (column 3, lines 3-15);
 - A power management system (14) configured to transition the device to the low power state (115) when a signal is detected on the bus (power usage request).

Oprescu fails to disclose a power supply, bus or CPU. Cromer discloses a system comprising:

- A power supply (240);

- A bus electrically connected to the power supply (208);
- A central processing unit in communication with the bus (200)

Cromer also discloses a system wherein the physical layer interface is a device connecting the bus to the network (Network).

The ability to modify the device and the power management system comes from Cromer's use of the general-purpose processor, which can be used to carry out the functions of the power manager and signal transmitter of Oprescu. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the device and the power management system. The motivation to modify is the space and power savings gained through the combination of these two elements.

- As per claim 22, Oprescu discloses a method comprising:
 - Within a networked computer system having an operating system (10), monitoring a bus that supplies power to a device (14) that includes a register, wherein the device is configured to include a high power state, a first low power state, and a second low power state (column 3, lines 3-15);
 - Writing data to the register by the operating system to indicate whether wake up of the device is enabled or disabled (It is inherent that information regarding whether wake up is enabled or disabled is stored when looking at 116. Lower priority requests to power up are disabled until all higher priority requests are granted.); and
 - Changing the power state of a device to the first or second low power state (115) when a signal is detected on the bus depending upon whether wake up of the device has been enabled (power usage request).

Oprescu fails to disclose that the device is a physical layer interface. Cromer discloses a method wherein the device is a physical layer interface. As discussed above in reference to claim 1, it would have been obvious to modify the teachings of Oprescu to include the physical layer interface in view of the teaching of Cromer. Motivation to modify arises from the improvement in performance gained through the use of a physical layer interface as outlined in Cromer.

- As per claim 30, Cromer and Oprescu, as described above, discloses an apparatus comprising a signal assertion causing a physical layer interface to switch to a low power state. Thus, Cromer and Oprescu also teach a computer program product residing on a computer readable medium for powering down a physical layer interface as a result of a signal asserted on the bus. The examiner takes Official Notice that storing a computer program product on a computer readable medium, such as a disk drive or a diskette, is a well known and generally accepted method of backing up a computer program product.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oprescu and Cromer, as applied above, and in view of US Patent No 6449677 to Olarig et al (Olarig).

- As per claim 3, Cromer discloses an apparatus wherein the bus is a PCI bus (208). Cromer fails to disclose a PCI-X bus being an art-identified equivalent of a PCI bus. Olarig discloses PCI and PCI-X buses as equivalent types of input/output buses (column 8, lines 7-9). It would have been obvious to one of ordinary skill in the art at the time of invention to substitute the PCI-X bus for a PCI bus as these devices are well known and generally accepted art equivalents.

Art Unit: 2116

5. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oprescu and Cromer, as applied above, and in view of US Patent No 6675356 to Adler et al (Adler).

- As per claim 20, Cromer discloses the system wherein the communication device is a local area network controller (230), but does not specify wireless LAN capability. Adler teaches a general network that may be any type of known network, including a wireless LAN (column 6, lines 58-61). It would have been obvious to one of ordinary skill in the art at the time of invention to substitute a wireless LAN device for a wired LAN device as these devices are well known and generally accepted art equivalents.

6. Claims 23, 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oprescu and Cromer, as applied above, and in view of US Patent No 6820171 to Weber et al (Weber).

- As per claim 23, Cromer discloses the system wherein the communication device is a local area network controller (230), but does not specify a Gigabit Ethernet device. Weber teaches a local area network that may be an Ethernet or a Gigabit Ethernet (column 6, line 66 – column 7, line 4). It would have been obvious to one of ordinary skill in the art at the time of invention to use a Gigabit Ethernet device as a LAN device, as a Gigabit Ethernet device is well known and generally accepted in the art.
- As per claim 31, Cromer discloses the computer program product wherein the communication device is a local area network controller (230), but does not specify a Gigabit Ethernet device. Weber teaches a local area network that may be an Ethernet or a Gigabit Ethernet (column 6, line 66 – column 7, line 4). It would have been obvious to one of ordinary skill in the art at the time of invention to use a Gigabit Ethernet device as a LAN device, as a Gigabit Ethernet device is well known and generally accepted in the art.

Allowable Subject Matter

7. Claims 4-5, 10-11, 13-14, 16-19, 21, 26-29, 32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments filed 3/7/05 have been fully considered but they are not persuasive. Applicant is arguing that the references used in the Non Final Rejection do not "teach or suggest a device having a *physical layer interface* [that] having multiple power states, let alone one that has at least three power states, a high state and a first and second low power state."

Examiner disagrees. In regards to the argument that neither reference teaches having at least three power states, examiner points to Oprescu column 3, lines 2-12. Oprescu acknowledges that it is a generally well known feature of devices to operate in "an inactive state, a wait...state and a fully operational state." In regards to the argument that the references do not teach a physical layer interface having multiple power states, Oprescu, as stated above, teaches a general device that can operate in numerous states. Cromer teaches that the device could be a network controller having a physical layer interface (234).

All rejections of claim limitations as filed prior to the Amendment filed 3/7/05 not argued in their entirety or substantively in the response to the prior Office Action have been conceded by Applicant and the rejections are maintained henceforth.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anand Patel whose telephone number is (571) 272-7211. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2116

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ABP



JOHN R. COTTINGHAM
PRIMARY EXAMINER